**Verilog code to implement BCD to Excess-3 using Behavioral stlye**

**Design Code:**

module bcd(input [3:0]i, output [3:0]y);

always@(i) y<=i+3;

endmodule

**Test Bench:**

module tb();

reg [3:0]i;

wire [3:0]y;

integer x;

bcd dut(i,y);

initial begin

    $monitor("@time %3d : when input is %b output is %b",$time,i,y);

    for (x=0; x <16; x=x+1) begin

    i=x;

    #5;

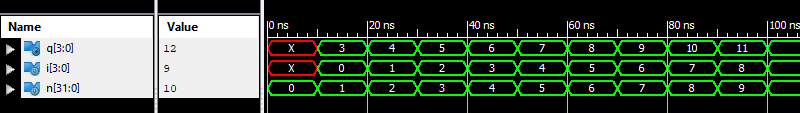
    end

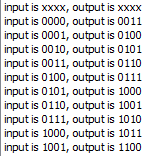
    $finish;

    end

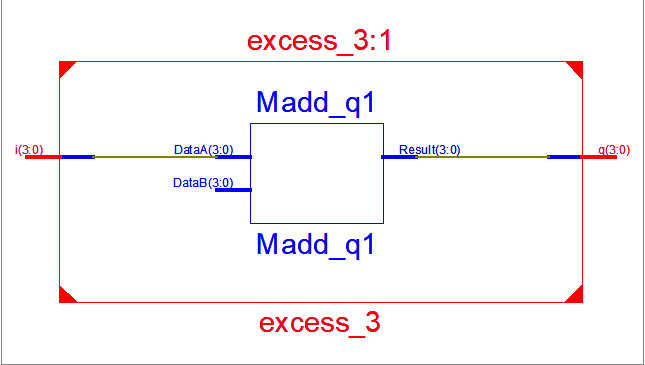
endmodule

**Simulation Result:**

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**RTL Diagram:**

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